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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,409	01/14/2004	Hirotaka Kawata	118006	2629

25944 7590 08/09/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,409	KAWATA ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *6,7 and 12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-11 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims 6-7, 12-14 drawn to an invention nonelected with traverse dated 07/17/05. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

2. The drawings were received on 15 July 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 8-11, 15, and 17 rejected under 35 U.S.C. 102(e) as being US 6528358 to Yamazaki et al.

Regarding claim 1, Yamazaki discloses a transistor in fig. 23E, comprising: at least a monocrystalline semiconductor layer 41, column 44 line 32, including a channel region 52, column 45 line 31, a lightly doped region 50, column 45 line 25, and a heavily

doped region 49, column 45 line 16, and a gate insulating film 38 provided over the monocrystalline semiconductor layer 41, the gate insulating film having a thermal oxide film 38, column 44 line 33, formed on the monocrystalline semiconductor layer 41 and at least one vapor-deposited insulating film 42, column 44 line 38, formed on the thermal oxide film 38, fig. 23B, the at least one vapor-deposited insulating film 42 covering an area including at least the channel region 52, the lightly doped region 50, and the heavily doped region 47 of the monocrystalline semiconductor layer 38, fig. 23E.

With respect to monocrystalline semiconductor layer, the interpretation of such layer is a material comprising a crystal structure or substantially single crystal structure. Suzawa (668628) discloses such interpretation, i.e, crystalline silicon is single crystal silicon in column 18 lines 61-63.

Regarding claim 2, Yamazaki discloses the transistor according to claim 1, the monocrystalline semiconductor layer 38 being made of monocrystalline silicon, column 44 line 33 and discussion in claim 1 above.

Regarding claim 3, Yamazaki discloses the transistor according to claim 1, the monocrystalline semiconductor layer 38 being a mesa type, Fig. 23A.

Regarding claim 4, Yamazaki discloses the transistor according to claim 1, the monocrystalline semiconductor layer 38 having a thickness of 50 nm, column 33 line 11.

Regarding claim 5, Yamazaki discloses the transistor according to claim 1, the thermal oxide film 38 of the gate insulating film having a thickness of 50 nm, column 33 line 18.

Regarding claims 8-11 and 15, Yamazaki discloses an electro-optical device, comprising: a transistor, fig. 23E, wherein a transistor according to claim 1 being provided as a switching element in a display area, fig. 60F, a electro-optical device, fig. 60E, a semiconductor device, 23E.

In the recitation 'an electro-optical device' and 'an electronic apparatus' has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478(CCPA 1951).

Regarding claim 17, Yamazaki discloses an active switching element, comprising; a monocrystalline semiconductor layer 41 having a surface and a side extending substantially perpendicular to each other; an insulating 38 covering both the surface and the side of the monocrystalline semiconductor layer 41, fig. 23A, the insulating film having a thermal oxide film 38 formed on the monocrystalline semiconductor layer 41; and at least one vapor-deposited insulating film 42 formed on the thermal oxide 38, fig. 23B.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6528358 to Yamazaki et al. in view of US 6653657 to Kawasaki et al.

Regarding claim 16, Yamazaki discloses the transistor comprising the monocrystalline semiconductor layer 441 further having a storage capacitor electrode portion 49, the thermal oxide film 38 and the vapor-deposited insulating 42 being interposed on the capacitor electrode portion 49 and serving as a dielectric, fig. 23E.

But Yamazaki does not disclose the transistor according to claim 1, further comprising: a capacitor line.

However, Kawasaki discloses a transistor comprising a capacitor line 235, fig. 10D, the semiconductor layer 208, fig. 9A, further having a storage capacitor electrode portion 221, fig. 10A, the oxide film 207, fig. 9A, being interposed between the capacitor line 235 and the storage capacitor electrode portion 221 and serving as a dielectric, fig. 10D. At the time the invention was made; it would

have been obvious to one of ordinary skill in the art to use the storage capacitor teaching of Kawasaki with Yamazaki's device, because it would have improved the operation performance and reliability of a semiconductor device as taught by Kawasaki in column 15 lines 34-40.

Response to Arguments

8. Applicant's arguments dated 15 July 2005 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a)..

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
02 Aug. 2005

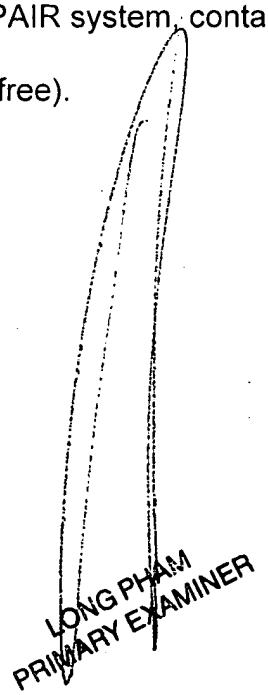

FIG. 15
RELATED ART

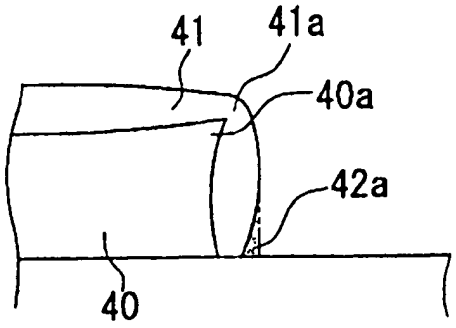

FIG. 16
RELATED ART

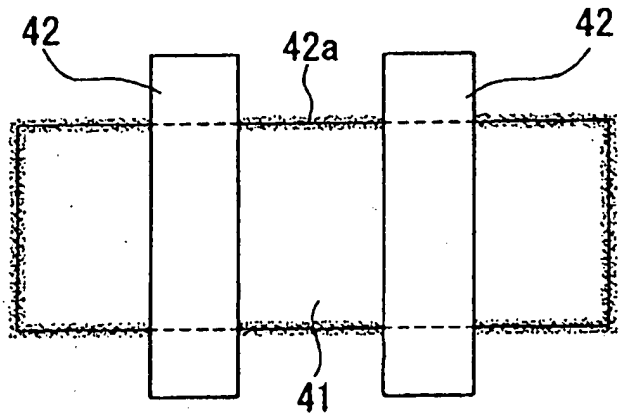

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FIG. 17
RELATED ART